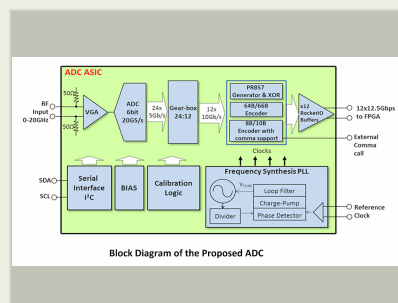
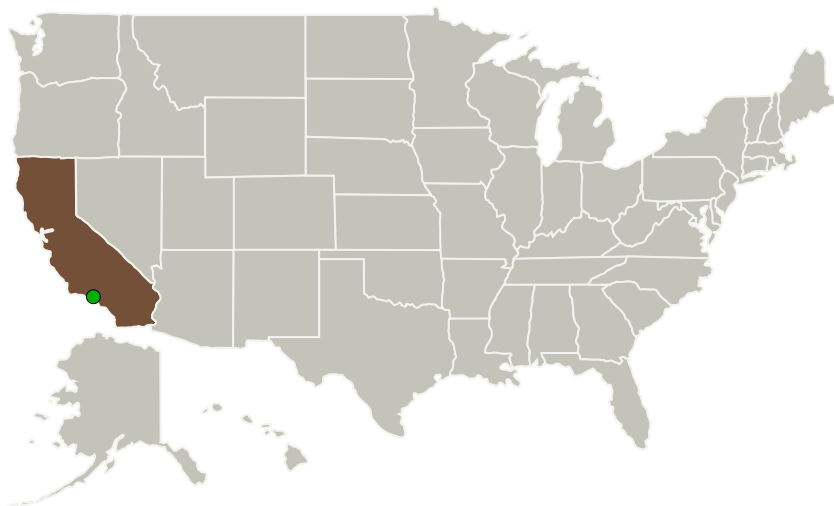


Project Introduction

The proposed project aims to develop a 20GSps 6-bit ADC required for microwave radiometers being developed for space and airborne earth sensing applications and radio telescopes. Aiming to improve performance and to reduce the size of the electronics, high resolution, high-sampling rate, power efficiency and low spur energy are required for ADCs employed for direct digitization. The proposed 20GS/s 6-bit time-interleaved successive approximation (SAR) ADC is intended to achieve >5 ENOB and 20GHz input bandwidth. A number of innovations will be introduced to the ADC in order to combine low power consumption with high signal to noise and distortion (SINAD), and spurious free dynamic range (SFDR). The proposed ADC will employ a novel timing calibration and interleave randomizing techniques which permit minimizing the peak energy of the spurs and increasing linearity. The proposed ADC chip will include a frequency synthesizer and a standard compliant configurable JESD204B interface for data exchange with an FPGA. The ADC will be implemented using a deep submicron CMOS technology. The project's Phase I confirmed the feasibility of implementing the proposed ADC. Phase II will include finishing design, fabrication, testing and delivering the ADC prototypes which will be ready for commercialization in Phase III.

Primary U.S. Work Locations and Key Partners



20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase II Briefing Chart Image

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20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase II

Completed Technology Project (2017 - 2019)



Organizations Performing Work	Role	Type	Location
Pacific Microchip Corporation	Lead Organization	Industry	Culver City, California
● Jet Propulsion Laboratory(JPL)	Supporting Organization	NASA Center	Pasadena, California

Primary U.S. Work Locations

California

Project Transitions

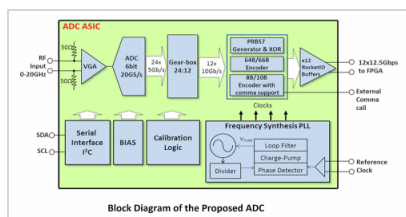
▶ **June 2017:** Project Start

✓ **October 2019:** Closed out

Closeout Documentation:

- Final Summary Chart(<https://techport.nasa.gov/file/140860>)

Images



Briefing Chart Image

20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase II Briefing Chart Image

(<https://techport.nasa.gov/image/127662>)



Final Summary Chart Image

20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase II

(<https://techport.nasa.gov/image/126208>)

Organizational Responsibility

Responsible Mission Directorate:

Space Technology Mission Directorate (STMD)

Lead Organization:

Pacific Microchip Corporation

Responsible Program:

Small Business Innovation Research/Small Business Tech Transfer

Project Management

Program Director:

Jason L Kessler

Program Manager:

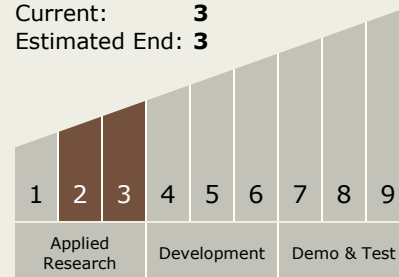
Carlos Torrez

Principal Investigator:

Denis Zelenin

Technology Maturity (TRL)

Start: 2
Current: 3
Estimated End: 3



20GSps 6-bit Low-Power Rad-Tolerant ADC, Phase II

Completed Technology Project (2017 - 2019)



Technology Areas

Primary:

- TX08 Sensors and Instruments
 - └ TX08.1 Remote Sensing Instruments/Sensors
 - └ TX08.1.4 Microwave, Millimeter-, and Submillimeter-Waves

Target Destinations

The Sun, Earth, The Moon, Mars, Others Inside the Solar System, Outside the Solar System